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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,415	09/20/2000	Kazuyuki Nakagawa	500-0-240	8537

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/665,415	Applicant(s) NAKAGAWA ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-10* is/are pending in the application.

4a) Of the above claim(s) *7-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Newly submitted claims 7-10, directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

A. Claims 1-3 are drawn to a semiconductor device, classified in class 257, subclass 780.

B. Claims 7-10, drawn to a method of making a semiconductor device, classified in class 438, subclass 613.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, method claims 7-10 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US Pat. 6455354).

Regarding claim 1, Jiang et al. disclose a semiconductor device comprising:

- a semiconductor element having a primary surface (112 in Fig. 6) with an element electrode (112 and 134 respectively in Fig. 6) and a back surface
- a circuit board/printed circuit board (PCB) having a primary surface (114 in Fig. 6) and a back surface with a board electrode (138 in Fig. 6), the circuit board having a predetermined opening hole (106 in Fig. 6)
- the primary surface of the element being bonded to the primary surface of the circuit board by means of an adhesive layer (108 in an embodiment as shown in Fig. 6), the adhesive layer being of the same size/width as that of the semiconductor element and smaller than that of the PCB
- the element electrode of the semiconductor element being connected to the board electrode provided on the back surface of the board via the opening hole
- the surrounding regions of the side surfaces and back surface of the semiconductor element on the circuit board being sealed with an encapsulate/resin to assume a tapered profile/structure (146 in Fig. 6), and
- the semiconductor element and the PCB directly contacting each other via the adhesive layer in order to provide increased contact area to relieve stress/tension between the semiconductor element and the PCB and to reduce flexing/twisting

- of the assembly and the encapsulation defects (Col. 5, line 35-45; Col. 8, line 22-27).

(Fig. 6; Fig. 1-6; Col. 7, line 50- Col. 8, line 60).

Jiang et al. fail to teach the adhesive layer being extended outward relative to and completely all the way around and extending outside the outer edge of the primary surface of the semiconductor element without reaching that of the circuit board.

Jiang et al. further teach (see an embodiment shown in Fig. 10) selecting a size and a configuration of the adhesive layer where the adhesive layer extends beyond the outer edge/edges of the semiconductor element (see 108 with respect to the die edges 128 in Fig. 10 being extended in width direction; Col. 9, line 10) without reaching that of the circuit board so that the visual inspection from the bottom surface can be performed and the encapsulation defects such as lodging of the filler particles at the edges/corners of the semiconductor element can be reduced for the device (Col. 9, line 5-12; Col. 7-9).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the adhesive layer extending outside the outer edges of the primary surface of the semiconductor element in all directions including length, width and radial directions such that the adhesive layer extends completely all the way around the primary surface of the semiconductor element without reaching that of the circuit board as taught by the embodiment of Fig. 10 in Jiang et al. so that the visual inspection can be performed from top and the bottom surfaces and alignment of the semiconductor

element on the PCB and the encapsulation defects at the edges/corners of the semiconductor element can be further reduced on top and bottom corner surfaces in Jiang et al's device.

Regarding claim 3, Jiang et al. teach substantially the entire claimed structure as applied to claim 1, wherein the surrounding regions of the side surfaces and back surface of the semiconductor element being sealed with the resin (146 in Fig. 6).

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US Pat. 6455354) in view of Taguchi et al. (US Pat. 6429372).

Regarding claim 2, Jiang et al. teach substantially the entire claimed structure as applied to claim 1, except the surrounding regions of the sealed resin to assume a flange structure.

Taguchi et al. teach using the sealing resin having surrounding regions (21 in Fig. 2) of the side surfaces of the semiconductor element on the circuit board being sealed with a resin to assume a chamfered flange structure to improve rigidity and stiffness for a device (Col. 10, line 10-48).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the surrounding regions of the sealed resin to

assume a flange structure as taught by Taguchi et al. so that the stress/tension between the semiconductor element and the PCB, the flexing/twisting of the assembly and the encapsulation defects can be reduced and rigidity can be improved in Jiang et al's device.

Response to Arguments

5. Applicant's arguments filed on 07-02-03 have been fully considered but they are not persuasive.

A. Applicant contends that the adhesive tape in Jiang et al. in Fig. 10 extends around the edges 128 of the die in Fig. 10 in one direction as shown in the cross sectional view, but not completely all the way around the die edges.

However, as explained above, Jiang et al. further teach selecting the size and configuration of the adhesive tape to improve the visual inspection and alignment and to reduce the filler particle lodging defects (see Col. 9, lines 5-8). It would have been obvious to one of ordinary skill in the art to select the adhesive layer being extended beyond both edges and completely around the die so that the visual inspection can be performed from top and the bottom surfaces, alignment of the die on the PCB can be improved and the encapsulation defects can be further reduced on the top and bottom surfaces of the PCB.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310

(Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

09-09-03

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800